SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MEMORY PRODUCTS TIMING SPECIFICATIONS

There has been for some years misunderstandings about the definition and specification of Memory timing parameters. Many companies have used different timing names and different waveform diagrams. Sometimes parameters are not clearly and unequivically defined.

Timing parameter names have historically tended to describe the functions of the time, for example:

– t_{AH} Address Hold time

– t_{DH} Data Hold time

– t_{ACC} Access time

These names do not describe very well the actual time specified, t_{AH} does not say hold time from what, to what. t_{ACC} does not specify whether this is the time from, for example, addresses valid or from chip enable asserted.

A better system is to follow that outlined by JEDEC. This uses both signal names and logic states to define the timing parameters.

The system follows the rules as in the example "t_{1234}", where 1 and 3 specify the signal names (negative logic signals eg. $\overline{E}$ are shown without the negation bar), for example:

– Q Data Output

– D Data Input

– E Chip Enable

– G Output Enable

– A Addresses

– W Write Enable

and, 2 and 4 specify the logic level as in Figure 2 and follows:

– H a Low to High transition to above a High level measurement threshold

– L a High to Low transition to below a Low level measurement threshold

– V valid signals, above High or below Low measurement levels

– X transition or invalid signals, signals that are possibly changing and are below a high level or above a low measurement level.

Figure 1. Signal Names

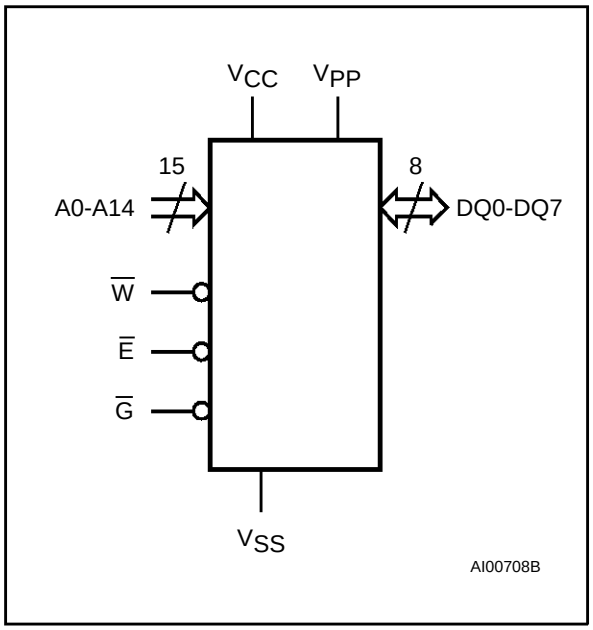
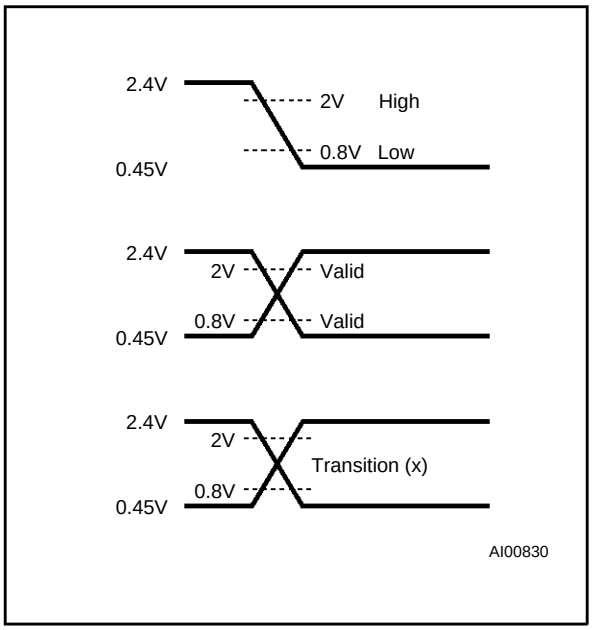


Figure 2. Input Output Waveforms References



Note: High. Low, Valid and Transition (X) levels.

Some examples of these definitions, with the name it replaces, are in Table 1.

Table 1. Timing Characteristics Example

Symbol	Alt	Parameter
t_{AVAV}	t_{RC}	Read Cycle Time
t_{AVQV}	t_{ACC}	Address Valid to Output Valid
t_{ELQX}	t_{LZ}	Chip Enable Low to Output Transition
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid
t_{GLQX}	t_{OLZ}	Output Enable Low to Output Transition
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid
t_{EHQZ}		Chip Enable High to Output Hi-Z
t_{GHQZ}	t_{DF}	Output Enable High to Output Hi-Z
t_{AXQX}	t_{OH}	Address Transition to Output Transition

Note: These are taken from the FLASH MEMORY data sheets.

MEASUREMENT CONDITIONS

The signal measurement conditions are also important for the definition of timings, there are three important definitions,

The input signal rise and fall time. Although, in theory, no timings depend on this - that is the definition of parameters is not dependant on the rise or fall time of the input signals - some products may have characteristics which vary with the slew rate of the input.

The levels of the input signal. Both the Low level and High level voltage. These obviously must be at least equal to the specified V_{IL} and V_{IH} for the device input signals.

The voltage level at which the timing measurement starts and stops.

For example, for EPROMs the SGS-THOMSON specification states:

– Input Rise and Fall times are 20ns max

– Input and Output signal levels are 0.4V(min) to 2.4V(max)

– Input and Output timing reference levels are 0.8V(Low) to 2.0V(High)

and, a signal is defined as Hi-Z (high impedance) when it is not driving or being driven.

USING THIS SYSTEM

The system then works, for example, like here after described.

A time specification of t_{AVQV} means a time from the point where the address lines are ALL below 0.8V for signals at or going to a logic Low level and above 2.0V for those at or going to a High logic level, to a time where the data output signals are ALL either below 0.8V or above 2.0V.

A time specification of t_{EHQZ} means a time from the chip enable input going above 2.0V to the point where the data output is no longer driving.

A time specification of t_{AXQX} means a time from the point where any single address line rises above or falls below its stable, valid level (0.8V for Low level or 2.0V for High level), to the point where any data output line transition passes these levels and is consequently no longer valid.

TIMING DIAGRAMS

The use of these definitions makes it unneccessary to draw the timing diagrams with times shown from a notional high or low measurement point, as the measurement points are clearly specified by the definition of measurement conditions and the signals and logic are described by the timing parameter description. The diagrams can be simplified for maximum clarity and understanding by indicating, diagrammatically, the timings from the waveform center point.

For example, if the measurement conditions for timing are specified as:

– Input Voltage levels are 0.45 to 2.4V

– Input and Output reference levels are 0.8 to 2V

and, Output Hi-Z is defined as the point where the signal is no longer driving; then in the diagram:

– t_{AVAV} is measured from the point where all address lines are either above 2V or below 0.8V to the same levels at the end of the cycle.

– t_{ELQV} is measured from $\overline{E}$ Low, or below 0.8V to the point where all data lines are either above 2V or below 0.8V.

– t_{EHQZ} is measured from $\overline{E}$ High, or above 2V, to where the data outputs are no longer driving the signal lines.

Note that the t_{ELQV} timing, for example, is shown diagramatically not from a "low" point on the $\overline{E}$ falling edge, but from the center and is shown not to a "high/low" point on the Data Output but again to the center. This is for clarity of the diagram, as the actual measurement points are clear from the definitions and timing names.

This system has been, or will be, adopted for all SGS-THOMSON Memory products.

Figure 3. Timing Diagram Example